**National Institute Of**

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**Assignment**

**Of**

**VLSI Circuit Design**

# Topic: Cmos Inverter

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## **Semester: 7th Semester**

## **Course Code: EC – 401**

Submission Date: 30.08.2024

Aim: The aim of this experiment is NMOS and PMOS Characteristics (transfer and output characteristics) and analysis using Cadence simulation software

**Tools Used**: Cadence Software

### Introduciton

Each transistor consists of a stack of a conducting gate, an insulating layer of silicon dioxide and a semiconductor substrate (body or bulk). Here PMOS and NMOS are connected with gates and drain shorted to each other. Side view is shown in figure 2.

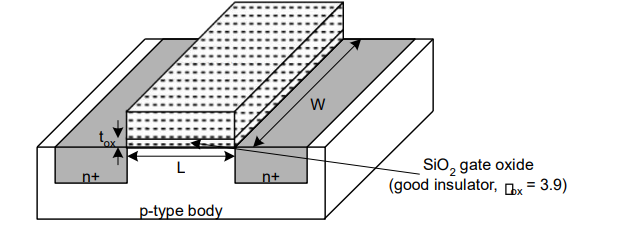


Fig: Basic MOS Transistor

The CMOS inverter is a basic building block for digital circuit design .As Figure 2 shows, the inverter performs the logic operation of A to Abar .When the input to the inverter is connected to ground, the output is pulled to VDD through the PMOS device M2 (and Ml shuts off). When the input terminal is connected to VDD, the output is pulled to ground through the NMOS device Ml (and M2 shuts off).The CMOS inverter has several important characteristics that are addressed in this lab: for example, its output Voltages wings from VDD to ground unlike other logic families that never quite reach the supply levels. Also, the static power dissipation of the CMOS inverter is practically zero, The inverter can be sized to give equal sourcing and sinking capabilities, and the logic Switching threshold can be set by changing the size of the device.

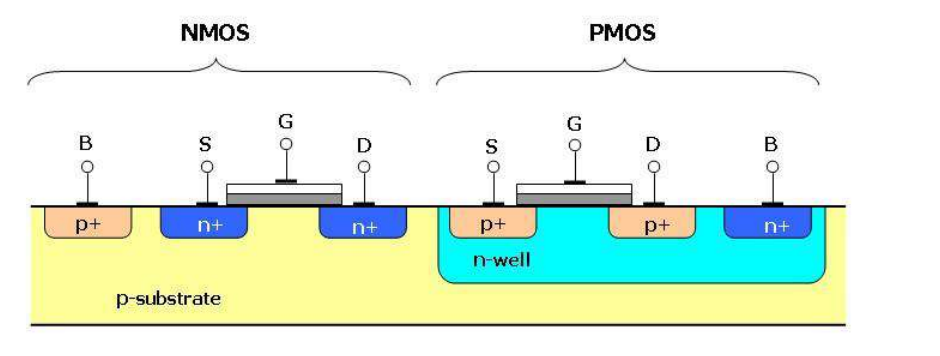


Fig Side view of CMOS Inverter

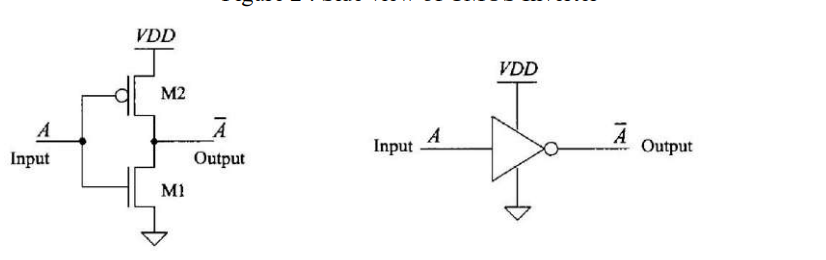
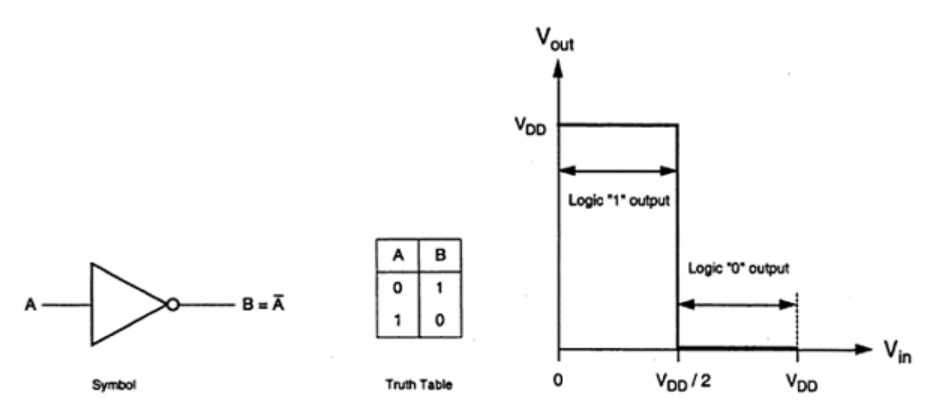


Fig CMOS Inverter, schematic and logic symbol

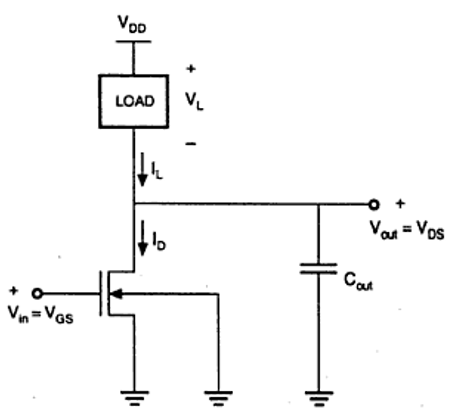
As the inverter shown in Figure.4 and the associated transfer characteristic plot. In Region1of the transfer characteristics, the input voltage is sufficiently low (typically less than the threshold voltage of Ml), so that Ml is off and M2 is on (Vsa »VTHP). As Vin is increased, both M2 and Ml turn on (region2). Increasing Vin further causes M2 to turnoff and Ml to fully turn on, as shown in region3

### principle of operationVC​(t)=Vin​e−RCt​

The logic symbol and truth table of ideal inverter is shown in figure given below. Here A is the input and B is the inverted output represented by their node voltages. Using positive logic, the Boolean value of logic 1 is represented by Vdd and logic 0 is represented by 0. Vth is the inverter threshold voltage, which is Vdd /2, where Vdd is the output voltage. The output is switched from 0 to Vdd when input is less than Vth. So, for 0<Vin<Vth output is equal to logic 0 input and Vth<Vin< Vdd is equal to logic 1 input for inverter



The characteristics shown in the figure are ideal. The generalized circuit structure of an nMOS inverter is shown in the figure below.



From the given figure, we can see that the input voltage of inverter is equal to the gate to source voltage of nMOS transistor and output voltage of inverter is equal to drain to source voltage of nMOS transistor. The source to substrate voltage of nMOS is also called driver for transistor which is grounded; so VSS = 0. The output node is connected with a lumped capacitance used for VTC

### nmosVC​(t)=Vin​e−RCt​

### Pmos

ϕ(f)=−arctan(2πfRC)

### circuit Design

1. **NMOS:**

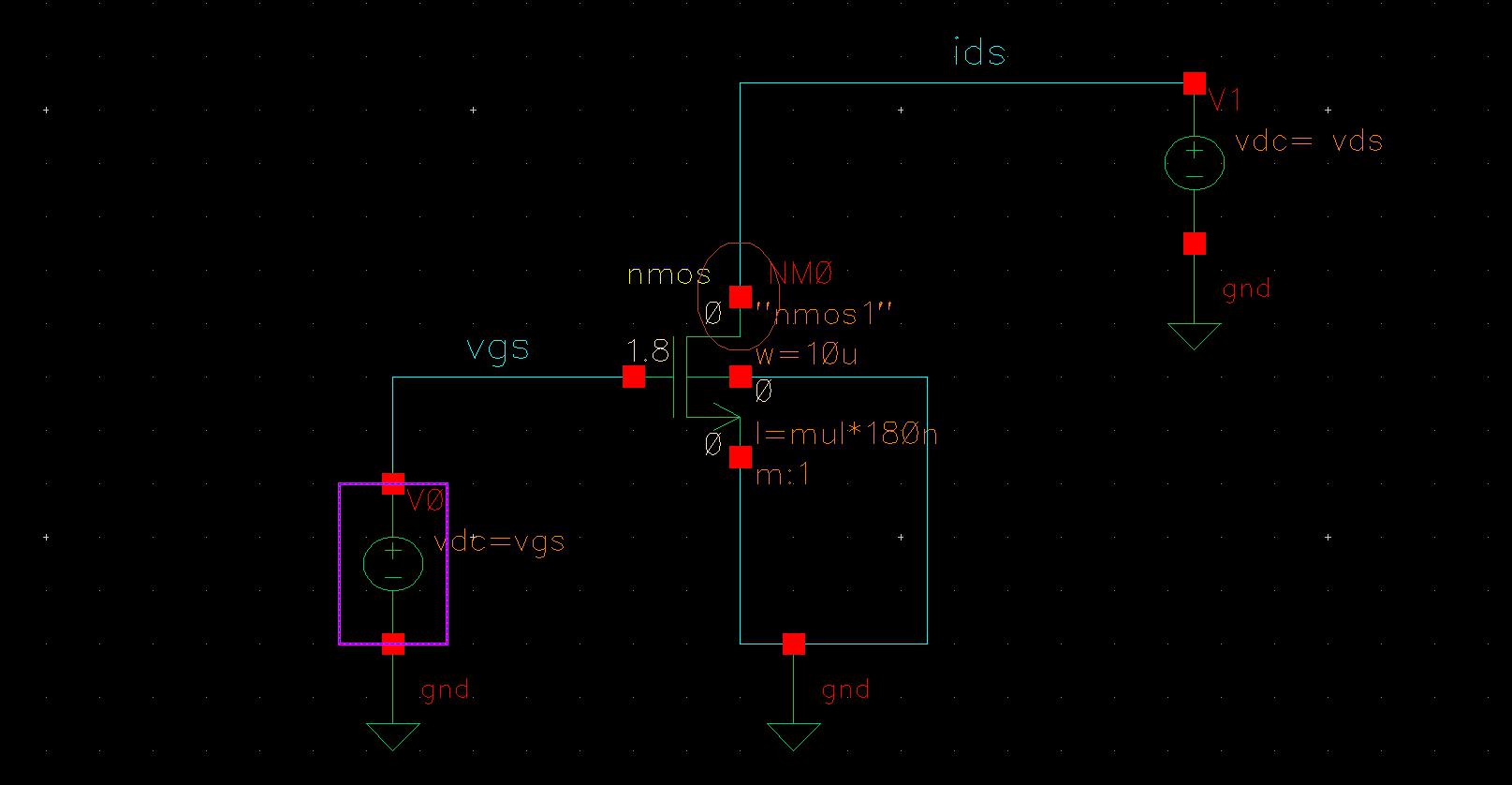


Fig: Circuit Diagram NMOS

* **Transfer Characteristics**

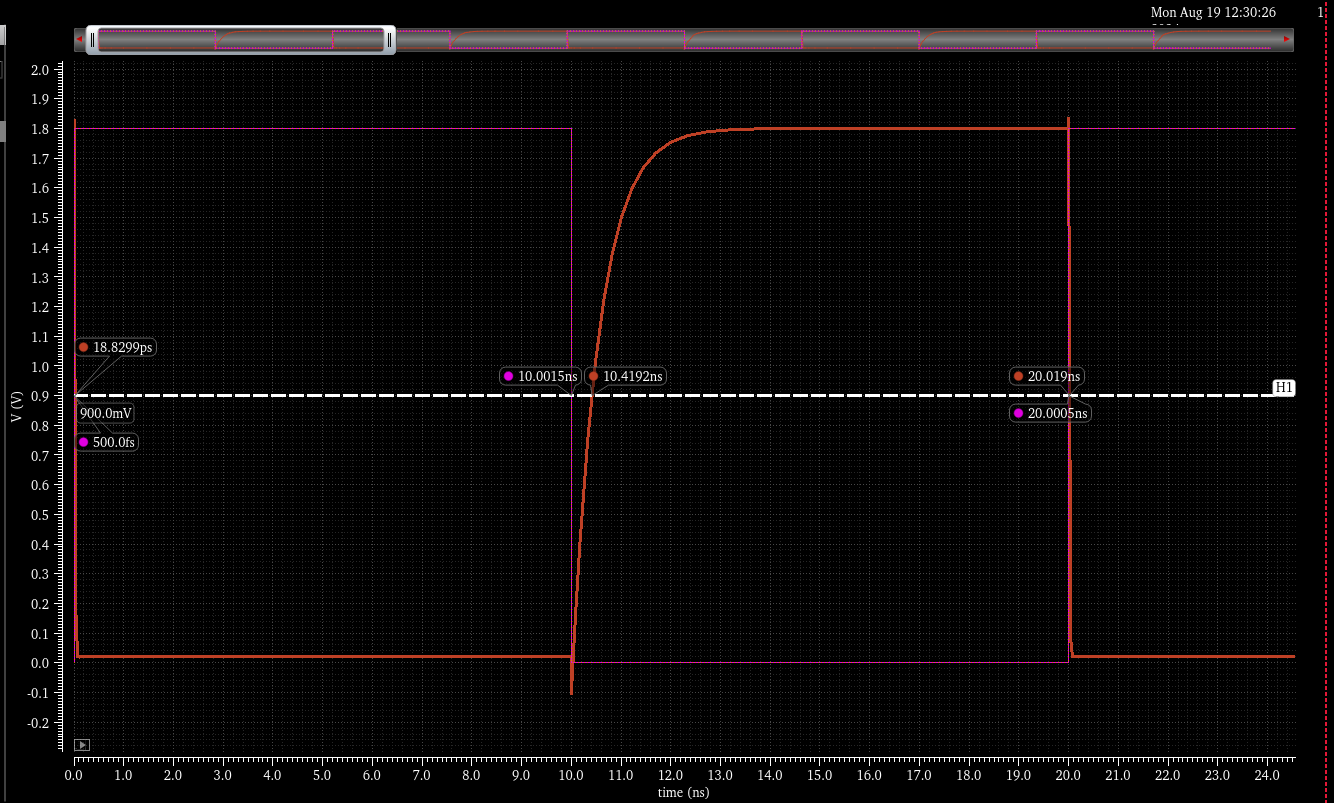


Fig: Propagation Delay for 5k resistance (NMOS)

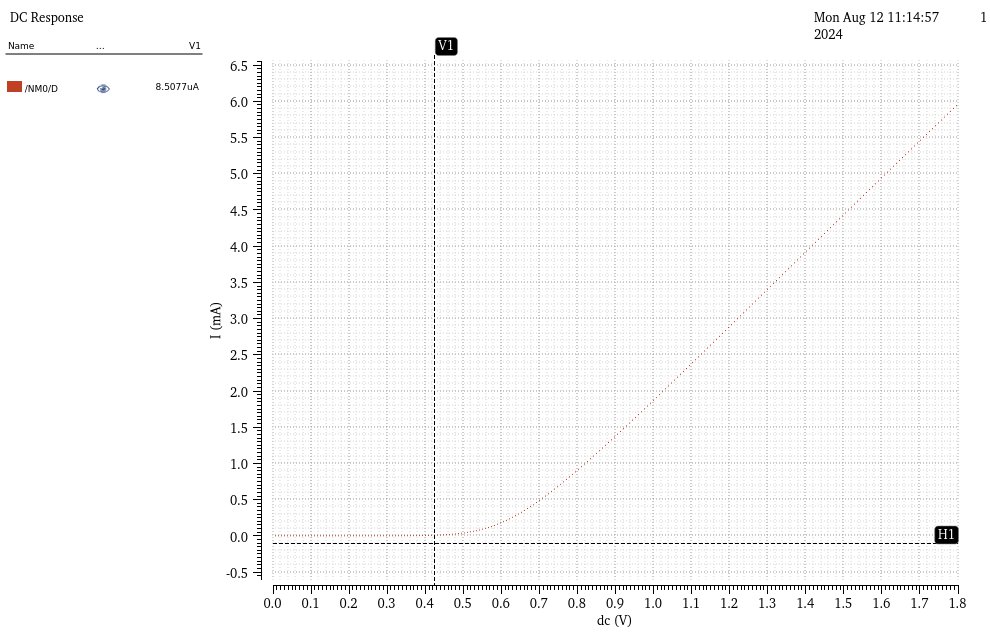


Fig: Id​ versus Vgs for different vds ( NMOS)

1. **PMOS:**

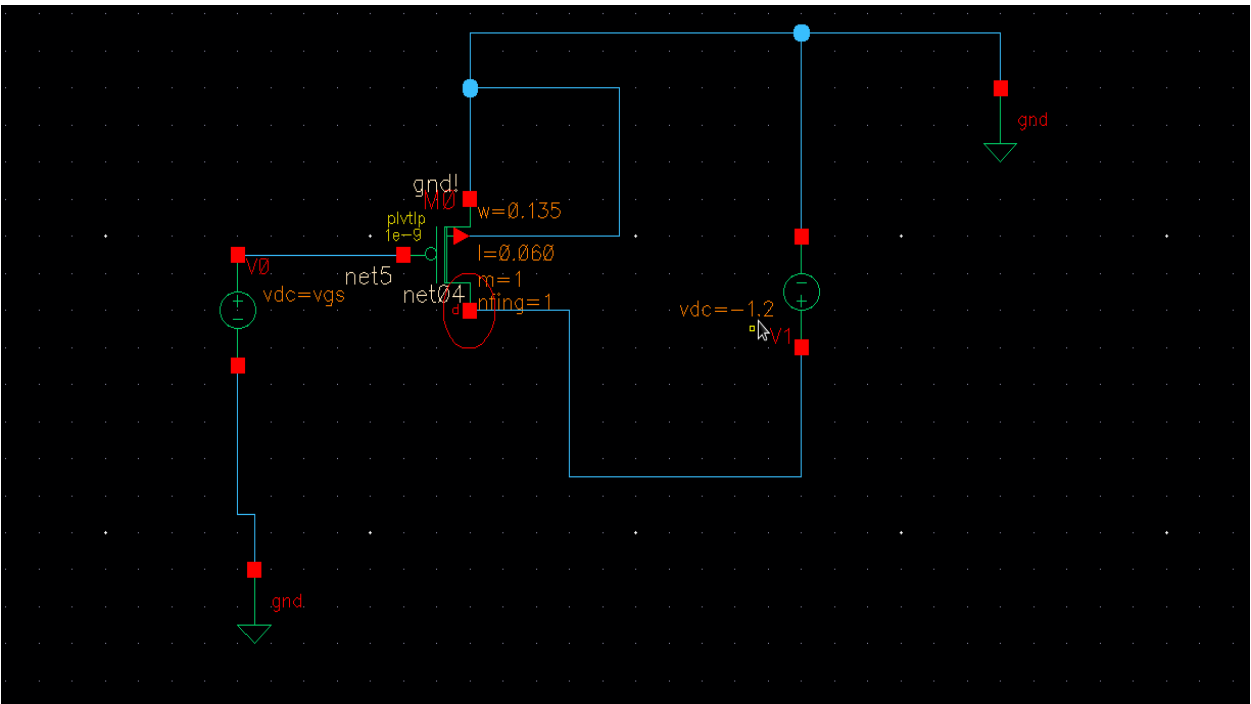


Fig: Circuit Diagram PMOS

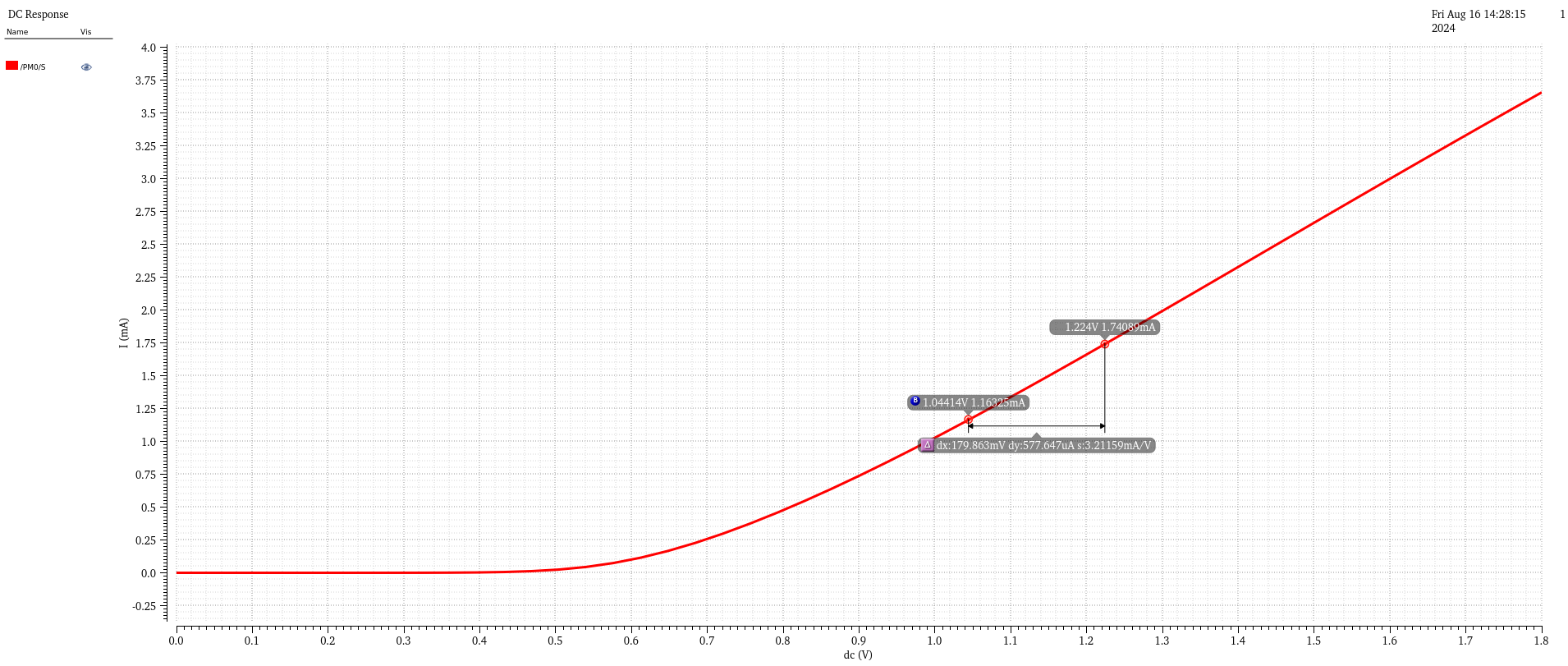


Fig: Ids versus Vsg for Vsd > Vth and calutation of Slope

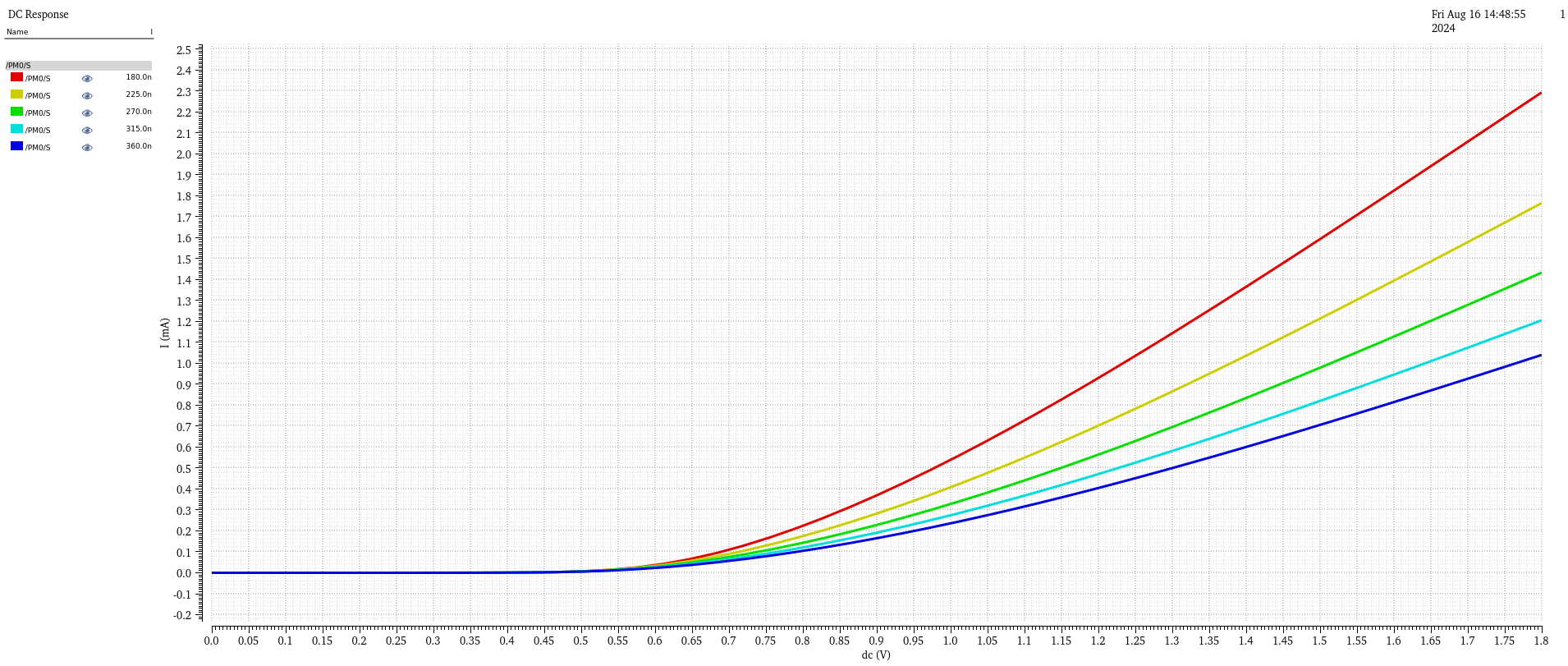


Fig: Ids versus Vsg for different values of Vsd > Vth

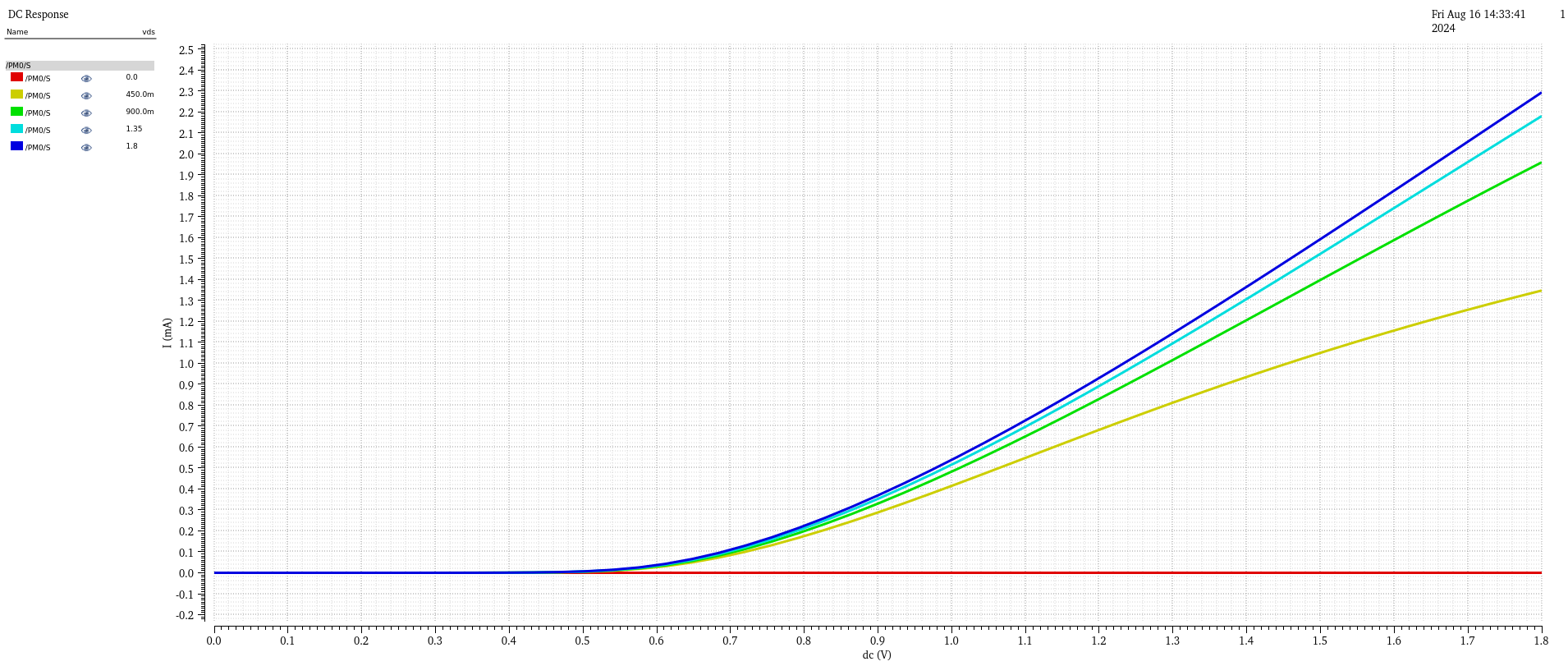


Fig: Ids versus Vsg for different values of Vsd > Vth and Vsd < Vth

* **Output Characteristics**

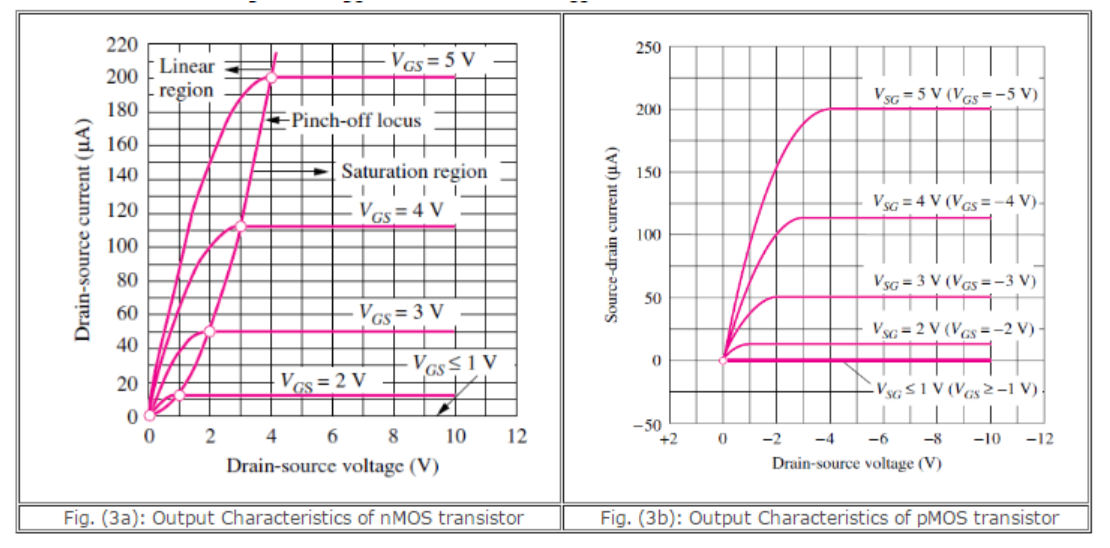
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Fig: Output Charcterstics (a) Nmos (b) PMOS

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1. **NMOS:**

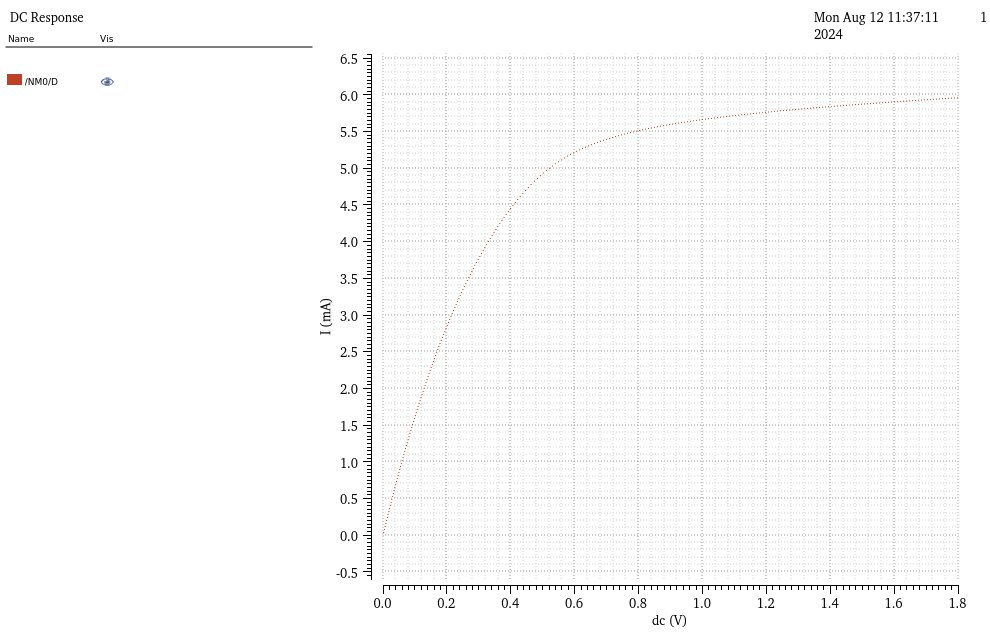


Fig: Id​ versus Vds NMOS

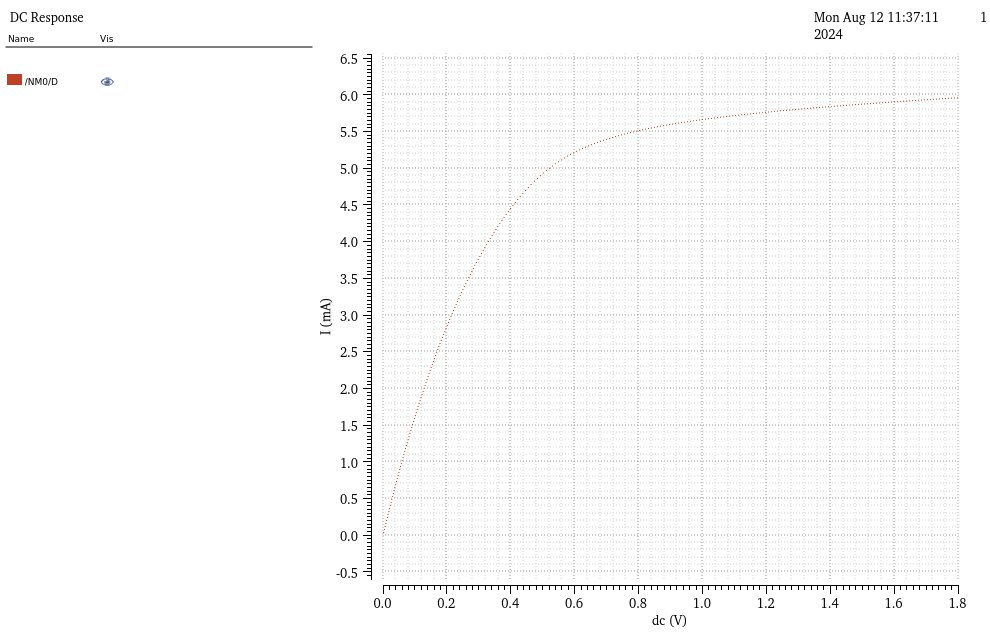


Fig: Id​ versus Vds for different vgs (NMOS)

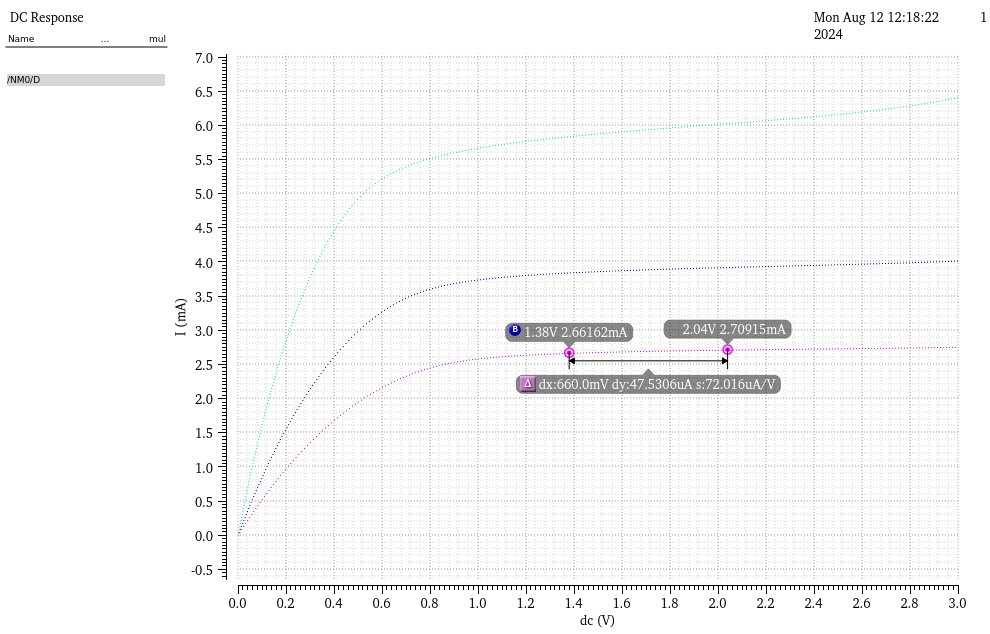


Fig: Id​ versus Vds for different vgs and length varition (NMOS)

1. **PMOS:**

* Plots Id​ versus Vsd​ for different Vsg values.

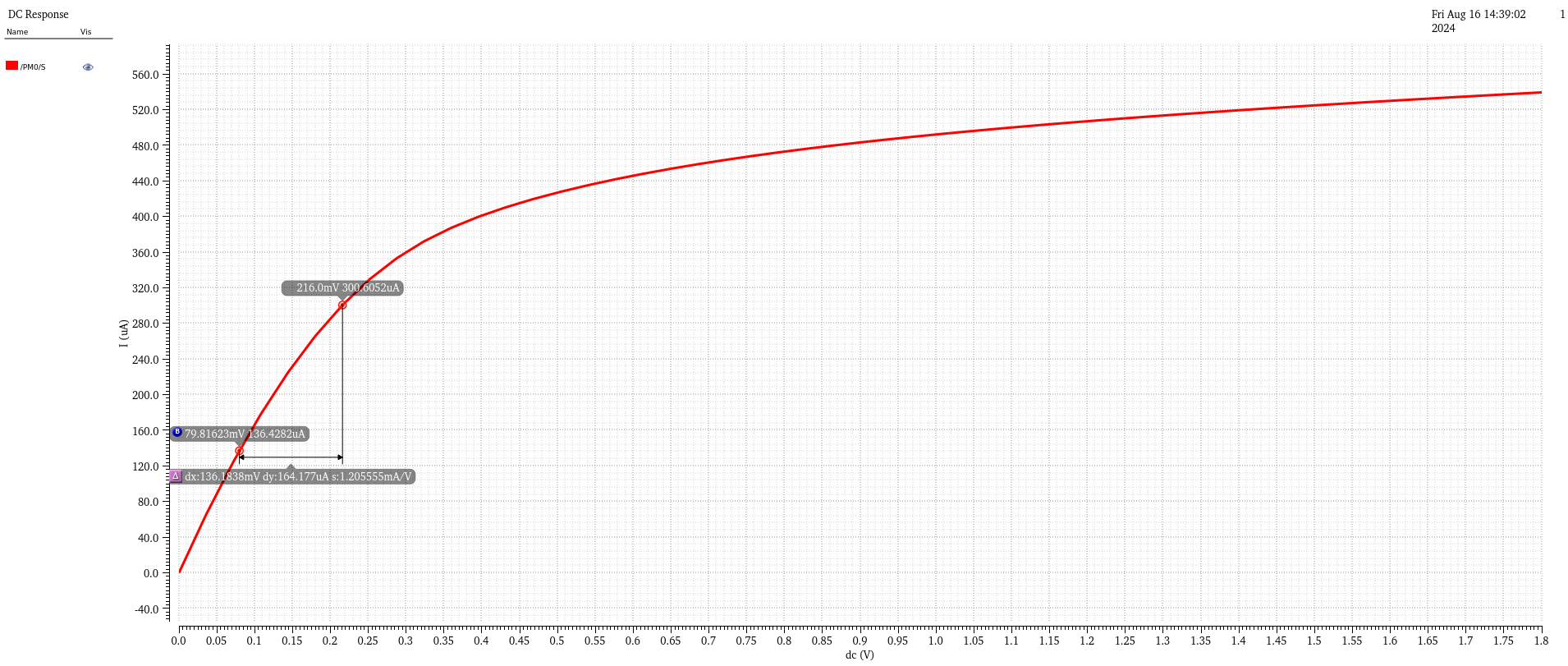


Fig: Ids versus Vsd​ for vgs > Vth

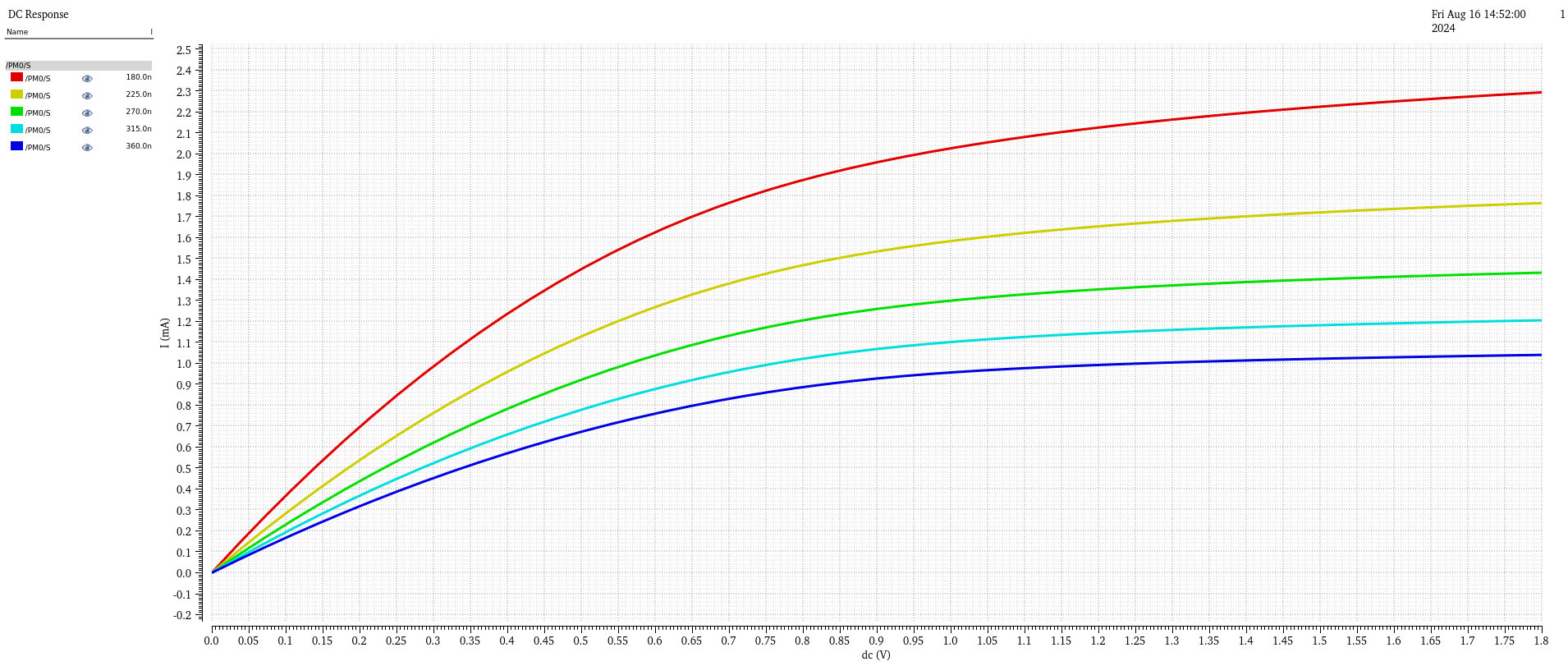


Fig: Ids versus Vsd​ for different value of vsg

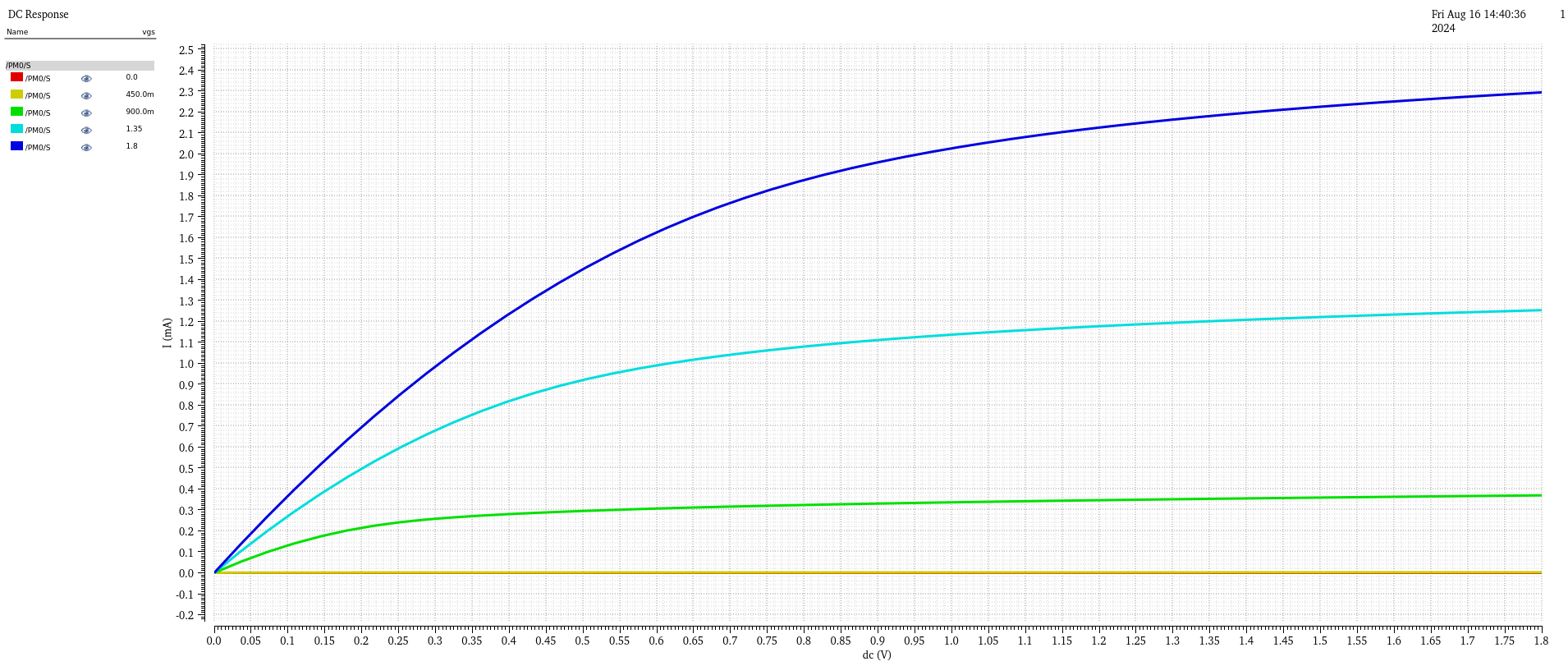


Fig: Ids versus Vsd​ for different value of vsg

### procedure

**1. Setup in Cadence:**

1. Open Cadence Virtuoso and create a new schematic for the NMOS and PMOS transistor circuits.
2. Add an NMOS transistor and a DC voltage source for VGS​ and VDS​.
3. Repeat the setup for the PMOS transistor with appropriate polarity for the voltage sources.
4. Connect the measurement probes to record the drain current Id and the gate voltage Vgs or Vsg​.

**2. Simulation of Transfer Characteristics:**

1. Set Vds​ to a constant value (e.g., 1.8V for NMOS and -1.8V for PMOS).
2. Sweep Vgs​ from 0V to the supply voltage for NMOS (or from 0V to the negative supply voltage for PMOS).
3. Run the simulation and plot Id versus Vgs​ to obtain the transfer characteristics.

**3. Simulation of Output Characteristics:**

1. Set Vgs​ to a constant value above the threshold voltage (e.g., 2.5V for NMOS and -2.5V for PMOS).
2. Sweep Vds​ from 0V to the supply voltage for NMOS (or from 0V to the negative supply voltage for PMOS).
3. Run the simulation and plot Ids versus Vds to obtain the output characteristics.

### Observations

1. **NMOS Transfer Characteristics:**
   * Threshold voltage Vth​ observed at approximately 0.7V.
   * Drain current ID​ increases quadratically with Vgs​ beyond Vth​.
2. **PMOS Transfer Characteristics:**
   * Threshold voltage Vth​ observed at approximately -0.7V.
   * Drain current ID​ increases quadratically with |VSG​∣ beyond |Vth​∣.
3. **NMOS Output Characteristics:**
   * In the linear region, ID​ increases linearly with Vds​.
   * In the saturation region, ID​ remains constant as Vds ​ increases.
4. **PMOS Output Characteristics:**
   * Similar behaviour to NMOS but with polarities reversed.
   * Id​ remains constant in the saturation region, decreases linearly in the linear region.

**1. Extracting NMOS Mobility (​):**

To determine the electron mobility for the NMOS transistor, use the following formula:

Where:

* Id is the drain current.
* is the oxide capacitance per unit area.
* ​ is the width-to-length ratio of the transistor.
* ​ is the gate-to-source voltage.
* is the threshold voltage.

**2. Extracting PMOS Mobility (​):**

For the PMOS transistor, the hole mobility is determined by:

Where:

* Id is the drain current.
* ​ is the oxide capacitance per unit area.
* ​ ​ is the width-to-length ratio of the transistor.
* VSG​ is the source-to-gate voltage.
* is the absolute value of the threshold voltage.

**3. Extracting Threshold Voltage ( ​):**

The threshold voltage can be extracted from the transfer characteristics using:

Where:

* Id is the drain current.
* is the electron mobility.
* is the oxide capacitance per unit area.
* is the width-to-length ratio of the transistor.
* ​ is the gate-to-source voltage.

**Example Calculations:**

1. **NMOS Mobility ():**

Suppose the following values are obtained from the simulation:

* + Drain current Id=2 mA
  + Gate-to-source voltage VGS=2.5 V
  + Threshold voltage Vth=0.7 V
  + Width-to-length ratio
  + Oxide capacitance Cox =1 fF/µm2 C

Plugging these values into the equation:

**2.PMOS Mobility (​):**

Assume similar values for the PMOS:

* Drain current ID=2 mA
* Source-to-gate voltage VSG=−2.5
* Threshold voltage ∣Vth∣=0.7 V
* Width-to-length ratio
* Oxide capacitance Cox =1 fF/µm2 C

Using the equation:

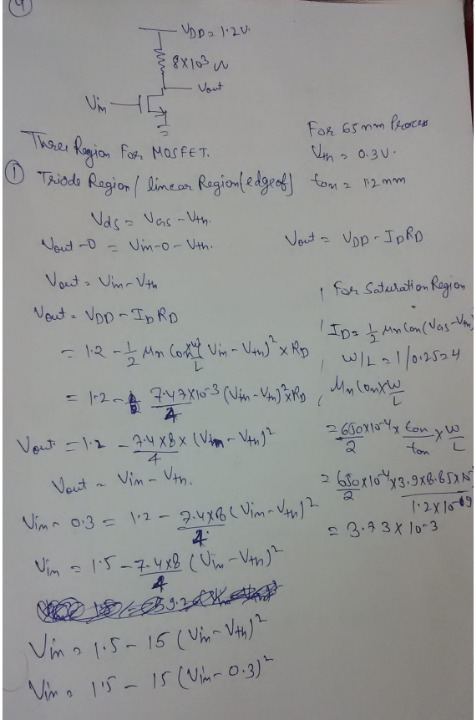
**3.Threshold Voltage Extraction (​):**

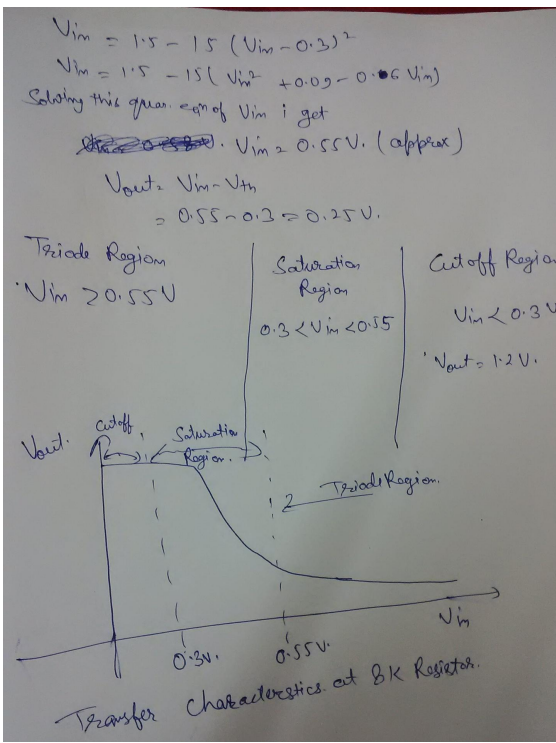
From simulation data:

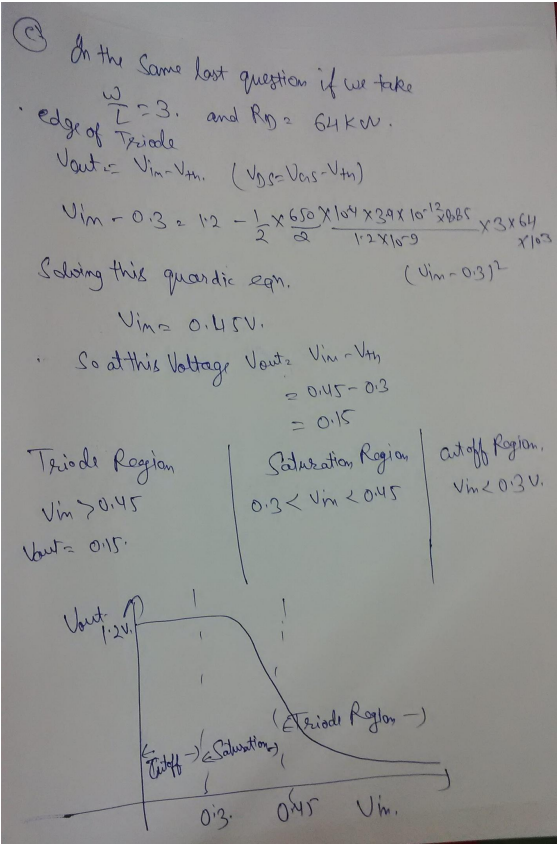
* Gate-to-source voltage VGS=2.5 V
* Drain current ID=2 mA
* Mobility μn=1.23×103 cm2/Vs
* Width-to-length ratio W\L=10
* Oxide capacitance Cox=1 fF/µm2

Calculating VthV\_{th}Vth​:

### Theoritical calculation







### conclusion

The experiment successfully demonstrated the transient and AC responses of an RC circuit using Cadence simulation software. The results for the transient response matched theoretical expectations, confirming the accuracy of the time constant and capacitor behaviour. The AC response analysis also aligned well with theoretical predictions, providing insights into the circuit's frequency response. The experiment reinforced the understanding of RC circuit dynamics and the utility of simulation tools in circuit analysis.

# References

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2. Sung –Mo Kang & Yusuf Leblebici, “CMOS Digital Integrated Circuits- Analysis & Designing”, MGH, Third Ed., 2003

3. John P Uyemura, “Introduction to VLSI Circuits and Systems”, Wiley India, 2006

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